REMARKS

Applicant respectfully requests reconsideration of the present application in view of the remarks below.

Claims 1 - 22 are pending in the application. Claims 1 – 12 are withdrawn. Claims 13-22 are rejected. Of these claims, claims 13 and 18 are independent claims, claims 14 – 17 depend either directly or indirectly from claim 13, and claims 19 – 22 depend either directly or indirectly from claim 18.

I. FORMAL MATTERS

Drawings

Applicants note with appreciation Examiner's acceptance of drawings submitted on February 13, 2008.

II. REJECTIONS UNDER 35 U.S.C. § 102 (a)

The Examiner has rejected Claims 13-22 under 35 U.S.C. 102(a) as being anticipated by Robertson W et al.: "RTL synthesis for systolic arrays". Proceedings of the international symposium on circuit and system (ISCS). CHICAGO, MAY 3-6, 1993, NEW YORK, IEEE, US, VOL 2, May 3, 1993, pages 1670-1673, XP010115439 ISBN: 0-7803-1281-3 (hereinafter "Robertson"). Applicants note that the Examiner cites Ashar as a basis for the rejection (see, e.g., page 2, part 2 of the Office Action) and assume that the Examiner refers to Robertson when citing Ashar.

Applicants traverse this rejection at least because Robertson does not disclose "a method of scheduling processing in a hardware threaded circuit, comprising . . . receiving information including processing element resources, a number of processing elements, and a window size corresponding to a number of downstream processing states to be examined," as set forth in claim 13.

The present invention is directed to a hardware threading mechanism providing temporary borrowing of unutilized pipeline stages from processing elements to boost throughput performance and/or to reduce the power consumption of tasks running on active processing elements (see application as-filed, specification at paragraph [0035]). For example, the hardware threading may include dynamic borrowing of available processing resources between interconnected processing elements (see application as-filed, specification at paragraphs [0006] and [0030], and claim 13).

Regarding claim 13, the Examiner directs Applicants' attention to Robertson at page 1671, col. 2 line 20 to 1672 col. 2 line 50. While Robertson mentions scheduling and resource allocation, Applicants submit that Robertson does not describe "a method of scheduling processing in a hardware threaded circuit, comprising . . . receiving information including . . . a window size corresponding to a number of downstream processing states to be examined", as set forth in claim 13. Instead, Robertson describes scheduling and resource allocation for a specific Register Transfer Level (RTL) systolic synthesis strategy and illustrates the strategy using a systolic unit for band-matrix multiplication (see Robertson, page 1671, col. 1, lines 31 – 35 and FIG. 1). Robertson describes constraints for implementing the synthesis strategy, including arrival rate, system clock period, time differences between valid data arrival at boundaries of systolic units, silicon area, and system delay. Applicants submit that the described synthesis strategy for scheduling and resource allocation, including the described constraints and implementation, is different than "receiving information including . . . a window size corresponding to a number of downstream processing states to be examined of the present invention," as set forth in claim 13. For example, the present invention may traverse downstream states in a schedule to look ahead by one or more states based on the window size (see application as-filed, e.g. the specification at paragraph [0063]). Future operations can be rescheduled earlier (such as within a current state) by maximizing the usage of underutilized resources.

Moreover, Robertson does not describe "receiving information including processing element resources" and "a number of processing elements", as set forth in claim 13. The present invention may use such information to schedule more operations within a current state of an unthreaded schedule (see application as-filed, specification at paragraph [0071]). For example, if a next state can be scheduled within a current state, such as when next state can be scheduled by borrowing an unused resource, the two states are scheduled together and the states are said to be threaded together.

Accordingly, Robertson does not describe "a method of scheduling processing in a hardware threaded circuit, comprising . . . receiving information including processing element resources, a number of processing elements, and a window size corresponding to a number of downstream processing states to be examined," as set forth in claim 13. Therefore, Applicants submit that claim 13 is patentably distinguishable over Robertson and request withdrawal of the art rejections. For at least the same reasons, Applicants submit that claims 14 – 22 are also patentably distinguishable over Robertson and request withdrawal of the art rejections.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue, or comment does not signify agreement with or concession of that rejection, issue, or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for withdrawing the prior art cited with regards to any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Applicants submit that the entire application is now in condition for allowance. Such action is respectfully requested at the Examiner's earliest convenience.

The Examiner is respectfully invited to telephone the undersigning attorney if there are any questions regarding this Response or this application.

Applicant does not acquiesce to any assertion made by the Examiner not specifically addressed herein.

The Assistant Commissioner is hereby authorized to charge payment of any additional fees associated with this communication or credit any overpayment to Deposit Account No. 500845, including but not limited to, any charges for extensions of time under 37 C.F.R. §1.136.

Respectfully submitted,

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